Subject:	Effective Date:	Initiated:
Electronics Pre-Operational Testing, Burn-in, and Spares	April 24, 2015	Tim Stevenson Office of Project Management
	Supersedes: **New**	**Approved:** Mike Williams Associate Laboratory Director for Engineering and Infrastructure

Management System (Primary):	03-Engineering
Management System Owner:	Associate Laboratory Director for Engineering and Infrastructure
Management Process:	03.04-Engineering Programs and Processes
Process Owner:	Associate Laboratory Director for Engineering and Infrastructure
Subprocess:	03.04.09- Approval of Electrical Equipment/Installations
Subprocess Owner:	Head, Electrical Engineering; Head, AC Power
Subject Matter Expert (SME):	Head, Project Management Office; Head, Electrical Engineering; Head AC Power

1.0 Applicability

This procedure describes the responsibilities and actions to be implemented for testing PPPL-designed electronics modules and subsystems prior to making them available for immediate use or placing in inventory as service or replacement spares.

2.0 Introduction

PPPL practices for in-house electronics module designs provide for reliable operation and long-term sustainability. This Standard is in place to continue and maintain the reliable operation of PPPL-designed and built electronics modules and captures PPPL design practices and provides a process to identify and remedy any parts or components that impact reliability and mitigate any effects on modules.

Parts selection and design review procedures sustains mean time between failures (MTBF) performance that supports operations by improving planning for spares procurement and testing of new builds, including planning and recommending burn-in times and procedures for new modules. Tracking of burn-in time will continue to be accomplished by use of normal operating logs and records. This standard documents that process and adds specification and documentation of burn-in time for new modules.

3.0 Reference Documents

- ENG-007 Rev 1 – Reliability, Availability, and Maintainability (RAM) Modeling and Apportionment

- ENG-010 - Control of Drawings, Software, and Firmware
- ENG-029 – Technical Definitions and Acronyms
- ENG-030 Rev 3 – PPPL Technical Procedures
- ENG-033 Rev 4 – Design Verification
- MIL-HDBK-217F – Military Handbook: Reliability Prediction of Electronic Equipment
- MIL-STD-883J CN 4 – Department of Defense Test Method Standard, Microcircuits, Method 1015.10: Burn-In Test

4.0 SCOPE

PPPL in-house electronics modules are defined here as electronic assemblies containing or consisting of one or more printed circuit cards and associated components and connectors, power supplies, chassis, etc. that make up a system component or functional block. An embedded processor and its associated firmware, memory and interfaces may be considered part of a larger system component or as a system component in itself at the discretion of the subsystem System Engineer. This Standard defines parts selection, testing procedures, and burn-in requirements, and designates where records are kept.

This standard is equally applicable to spares and inventory modules, as well as modules in service.

5.0 STANDARD

5.1 Design Practice

The System Engineer shall, as part of the development, design and parts selection process,

- Specify and use Commercial, Industrial or Military grade parts and components in PPPL electronics designs whenever possible, and
- Identify any Unknown grade parts[1] and components and provide additional inspection, burn-in, and post-PTP surveillance to mitigate any effect on reliability of in-house electronics modules.

The System Engineer for each electronics module shall identify the estimated failure rate of the module, which shall be incorporated into PPPL system reliability modeling and planning, such as spares procurement and planning.

5.2 PTP Practice

The COG shall note the total burn-in time for modules tested in each PTP in the signature copy of the applicable PTP. Burn-in times as logged will be the best-effort figures from normal operating logs such as the Instrumentation and Control (I&C) log[2] and records. If a paragraph of the PTP in force at the time of testing for recording burn-in time is not present, the burn-in times shall be recorded in the Notes section of the signature copy.

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[1] Unknown grade parts are parts that have no manufacturer logo or name on the part, or which have no code date or lot number on the part even with manufacturer identification.

[2] The I&C log home page is on the internal PPPL network at http://nstx-ic-log.pppl.gov/

5.3 Post-PTP Surveillance when Unknown Grade1 Parts are Used

Post-PTP surveillance consists of tracking the subsystems that use Unknown grade parts and, if such a system fails and the failure is tracked to the Unknown grade semiconductor, the entire buy of that Unknown grade part is discarded and replaced with a new buy. In an emergency, existing spares from the same buy can be used for repair until replacement parts arrive.

5.4 Build and Test Practice

Parts selection should always use Commercial, Industrial, Automotive, or Military[3] grade parts whenever possible. These parts are qualified for reliability by the vendor in accordance with appropriate standards.

In the event that electronic components with no markings that identify the manufacturer and code date or lot number[4], then burn-in and post-PTP surveillance requirements for the component and the card are modified to ensure reliability of the module.

5.5 Burn-In Practice

Table 1 illustrates the characteristics of Power-On, Functioning, and Thermal Burn-In. MIL-HDBK-217 defines reliability of some components, such as processor CPUs, CPGAs, line or bus drivers and receivers, and display drivers, in terms of junction temperature. The junction temperature of some components is unchanged when signals are present; Power-On burn-in is stipulated for assemblies that contain only such semiconductor components. Assemblies or subsystems that contain components that have signal-dependent junction temperature shall be burned in using operating conditions, e.g. signals shall be present, real or simulated, that cause normal operating junction temperatures during burn-in; this is Functioning burn-in. Data may be real, simulated, or nominal waveform from signal generators as determined by the System Engineer.

Burn-in times include testing and evaluation time during prototype development or production. Credit for burn-in time begins with the last installed or replaced part installation in the subassembly or subsystem.

5.6 Burn-In and Surveillance under Installed Environmental Conditions

Some PPPL electronics subsystems are operated in elevated temperatures. Burn-in of these components will be done at temperatures that are a best effort match to operating temperatures.

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[3] Electronic parts are graded by the temperature range over which their specifications certify them for proper operation: Military, -55 C to +125 C, industrial grades such as Automotive, 0 C to +125 C or Industrial, -25 C to +85 C; Commercial, 0 C to 70 C.

[4] Electronic components that are not traceable to manufacturer production lots with known testing and burn-in documentation are classified as Unknown grade parts by industry standard practices as described in MIL-HDBK-217 and elsewhere. Use of these parts requires additional board burn-in time to ensure reliability of assemblies in which they are used.

Table 1. Burn-In Practices

Burn-In	Level	Requirement	Minimum Burn-in Time
Power On (no data throughput)	Board, Assembly, Chassis	Logic, Memory, Discrete, SSI/MSI Integrated Circuits	24 hrs (See Text)
Functioning (with data throughput)	Board, Assembly, Chassis	CPU, FPGA, Driver/Receiver	4-8 hrs (Higher when Unknown grade parts are used; See Text)
Thermal	Component	Reduced Life Testing Time	Parts Vendor, not PPPL Activity; See Text

Thermal burn-in is described in MIL-STD-883J, Method 1015.10: Burn-In Test, Test condition F: Temperature-accelerated test. This test procedure is intended to be specified for the vendor of the semiconductor component to apply to a sample of the production run as part of the certification of the parts in that run. This is a "thermally accelerated life test" and may be considered destructive testing, and is thus applied to samples from a production run and not applied to all parts.

In the event that a PPPL design must use a semiconductor component that is classified as Unknown (i.e. no vendor ID and code date or lot number on the part and thus no vendor-supplied failure rate or MTBF), the Post-PTP Surveillance process given above will be used.

5.7 Tracking of Burn-In and Surveillance Time

New builds shall be burned-in under Power-On or Functioning conditions to bring the total burn-in time up to the total specified in Table 1. Prototype bench time, beginning with the last parts insertion or substitution, is included in burn-in time.

Time in-situ prior to and during PTP procedures will be credited as burn-in and surveillance time. Time in service will be credited as post-PTP surveillance time.

Post-PTP operating time and failures should be tracked to approximately 1000 hours for each subsystem using normal operating logs per COG discretion.

Burn-In and Surveillance time will be logged at the conclusion of each PTP, including the system qualification and go-ahead at the beginning of each day when running shots is planned. The PTP signature copy will include the total amount of burn-in time at the conclusion of testing.

5.8 Critical Protection Systems

Some systems such as DCPS, and subsystems such as PCS, are deemed Critical Protection Systems because an undetected failure can damage the coils, power supplies, or other portions of NSTX-U.

The burn-in time for Critical Protection Systems will be 48 hours.

5.9 Firmware Practice

When a module uses firmware, certification testing records shall include identification of the firmware version and location of the source code and compiler.

When firmware is updated, either all cards in service and inventory shall be upgraded and tested with the new version, or the cards using different versions of the firmware shall be tracked, at the discretion of the System Engineer.

When firmware for a card is updated, the card and the assembly in which it is embedded will be certified with a new PTP at the functional level but new hardware electrical testing is not required.

5.10 Software Practice

Software PTP certification is attached to a given compilation build. The software that is certified by the PTP is characterized and tracked by checksum and the date and time of the binary executable file. When software is updated, including compilation with a different compiler, or whenever the checksum or file date and time for the binary executable changes, the software will be certified with a new PTP.

5.11 Repair and Failure Tracking and Records Repository

Parts used in repair shall be Commercial, Industrial or Military grade parts and components whenever possible. When Unknown grade parts or components are used, test and burn-in procedures specified by the System Engineer shall be implemented, with extended surveillance.

Repair log roll-ups or summaries shall be included with the PTP or other test record certifying the card or module for service. Documentation may be kept by COG or System Engineer, in the Ops Center or in the Project Files.

6.0 COG and System Engineer Discretion

The System Engineer for the relevant module or subsystem or the COG in charge of a PTP has the discretion to determine burn-in times, parts selection, testing and qualification, and burn-in times, and designation of the repository of repair and burn-in logs.